What is claimed is:

1. A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port so that the output voltage is indicative of a local time-average maximum of the input signal voltage.

2. The circuit as set forth in claim 1, wherein in steady state the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary.

3. The circuit as set forth in claim 1, wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

4. A method to provide an output voltage indicative of a local time-average maximum of an input signal voltage, the method comprising:

providing a field-effect transistor (FET) having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to an input port, and the second terminal is connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port.

5. The method as set forth in claim 4, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

6. A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to the input port, wherein the second terminal has a DC offset correction voltage; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

7. A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port so that the output voltage is indicative of a local time-average minimum of the input signal voltage.

8. The circuit as set forth in claim 7, wherein in steady state the FET is coupled to operate in a sub-threshold region if the average voltage is stationary.

9. The circuit as set forth in claim 7, wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

10. A method to provide an output voltage indicative of a local time-average minimum of an input signal voltage, the method comprising:

providing a field-effect transistor (FET) having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to an input port, and the gate and the second terminal are each connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port.

11. The method as set forth in claim 10, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width.

12. A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to the input port, wherein the gate and

the second terminal are connected to each other and have a DC offset correction voltage; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

13. A circuit comprising:

an input port;

an output port;

a first field-effect-transistor (FET) having a first terminal connected to the input port, a second terminal connected to the output port, and a gate connected to the input port; and

a second FET having a first terminal connected to the output port, a gate connected to the output port, and a second terminal connected to the gate of the first FET.

14. The circuit as set forth in claim 13, wherein the first FET has a device width, wherein the first FET has a leakage current in excess of 1 micro ampere per micron of device width of the first FET.

15. The circuit as set forth in claim 14, wherein the second FET has a device width, wherein the second FET has a leakage current in excess of 1 micro ampere per micron of device width of the second FET.

16. The circuit as set forth in claim 15, the input port having an input signal voltage, the output port having an output voltage, the circuit further comprising a direct current (DC) offset correction unit responsive to the output voltage to subtract the output voltage from the input signal voltage.

17. The circuit as set forth in claim 13, the input port having an input signal voltage, the output port having an output voltage, the circuit further comprising a direct current (DC) offset correction unit responsive to the output voltage to subtract the output voltage from the input signal voltage.

18. The circuit as set forth in claim 17, further comprising a capacitor connected to the output port.

19. The circuit as set forth in claim 13, further comprising a capacitor connected to the output port.

20. A method to provide a local time-average of an input signal voltage, the method comprising:

providing the input signal voltage to an input port;

providing a first field-effect-transistor (FET) having a gate connected to the input port, a first terminal connected to the input port, and a second terminal connected to an output port;

providing a second FET having a gate connected to the output port, a first terminal connected to the output port, and a second terminal connected to the gate of the first FET; and

sampling the average voltage at the output port.

21. The method as set forth in claim 20, further comprising providing a capacitor connected to the output port.